S/N Unknown PATENT

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Michael S. Briner

Examiner:

Unknown

Serial No.: Filed:

Unknown Herewith Group Art Unit:
Docket:

Unknown 703.007US8

Title:

READ-BIASING AND AMPLIFYING SYSTEM

## INFORMATION DISCLOSURE STATEMENT

MS Patent Application Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 et. seq., the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement.

Pursuant to 37 C.F.R. §1.98(d), copies of the listed documents are not provided as these references were previously cited by or submitted to the U.S. Patent Office in connection with Applicant's prior U.S. application, Serial No. 10/352431, filed on January 28, 2003, which is relied upon for an earlier filing date under 35 U.S.C. §120.

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

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Date of Deposit: February 25, 2004

Date 25 FM 104

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to The Commissioner for Patents, Mail Stop Patent Application, P.O.Box 1450, Alexandria, VA 22313-1450.

PTC/SB/08A(10-01)
Approved for use through 10/31/2002, OMB 651-0031
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Substitute for form 1449A/PTO Complete if Known INFORMATION DISCLOSURE **Application Number** Unknown STATEMENT BY APPLICANT Even Date Herewith Filing Date (Use as many sheets as necessary) Briner, Michael **First Named Inventor Group Art Unit** Unknown **Examiner Name** Unknown Attorney Docket No: 703.007US8 Sheet 1 of 4

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**DATE CONSIDERED EXAMINER** 

Substitute for form 1449A/PTO Complete if Known INFORMATION DISCLOSURE **Application Number** Unknown STATEMENT BY APPLICANT Even Date Herewith Filing Date (Use as many sheets as necessary) **First Named Inventor** Briner, Michael **Group Art Unit** Unknown Unknown **Examiner Name** Attorney Docket No: 703.007US8 Sheet 2 of 4

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**EXAMINER** 

**DATE CONSIDERED** 

PTC/SB/084(10-01)
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US Patent & Trademark Office U.S. DEPARTMENT OF COMMERCE
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**DATE CONSIDERED EXAMINER** 

COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: Unknown Filing Date: Herewith

Title: READ-BIASING AND AMPLIFYING SYSTEM

Page 1 Dkt: 703.007US8

S/N Unknown PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Michael S. Briner Examiner: Unknown

Serial No.: Unknown Group Art Unit: Unknown

Filed: Herewith Docket: 703.007US8

Title: READ-BIASING AND AMPLIFYING SYSTEM

## **COMMUNICATION CONCERNING RELATED APPLICATION(S)**

MS Patent Application Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Applicant would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

Serial/Patent No. 08/386704 5526364	Filing Date February 10, 1995	Attorney Docket 703.004US1	Title APPARATUS FOR ENTERING AND EXECUTING TEST MODE OPERATIONS FOR MEMORY
08/387018 5627786	February 10, 1995	703.005US1	PARALLEL PROCESSING REDUNDANCY SCHEME FOR FASTER ACCESS TIMES AND LOWER DIE AREA
08/826241 5,808,946	March 27, 1997	703.005US2	PARALLEL PROCESSING REDUNDANCY SCHEME FOR FASTER ACCESS TIMES AND LOWER DIE AREA
08/804,951 5,862,077	Feb. 24, 1997	703.007US1	FAST SENSING AMPLIFIER FOR FLASH MEMORY
08/895,618 5,835,411	July 17, 1997	703.007US2	Computer including a fast sensing amplifier
08/893,282 5,757,697	July 15, 1997	703.007US3	Method for sensing the binary state of a floating-gate memory device

COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: Unknown

Filing Date: Herewith

Title: READ-BIASING AND AMPLIFYING SYSTEM

Page 2 Dkt: 703.007US8

09/136,909 6,108,237	Aug. 20, 1998	703.007US4	FAST SENSING AMPLIFIER FOR FLASH MEMORY
09/642953 6,525,967 08/386688 5,682,496	August 21, 2000 February 10, 1995	703.007US5 703.008US1	FAST SENSING AMPLIFIER FOR FLASH MEMORY FILTERED SERIAL EVENT CONTROLLED COMMAND PORT FOR FLASH MEMORY
08/908242 6578124	August 7, 1997	703.008US2	SERIAL COMMAND PORT METHOD, CIRCUIT, AND SYSTEM INCLUDING MAIN AND COMMAND CLOCK GENERATORS TO FILTER SIGNALS OF LESS THAN A PREDETERMINED DURATION
09/401886 6581146	September 23, 1999	703.008US3	SERIAL COMMAND PORT METHOD, CIRCUIT, AND SYSTEM INCLUDING MAIN AND COMMAND CLOCK GENERATORS TO FILTER SIGNALS OF LESS THAN A PREDETERMINED DURATION
10/352419	January 28, 2003	703.007US6	INTEGRATED CIRCUIT WITH FEEDBACK
10/352431	January 28, 2003	703.007US7	FEEDBACK BIASING INTEGRATED CIRCUIT

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Date of Deposit: February 25, 2004

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